ABSTRACT

A transfer schedule SA and a transfer schedule SB for an A lot and a B lot different from each other are generated on a transfer control table, the succeeding transfer schedule SB is moved ahead in the direction of a time axis within a range over which it does not interfere with the transfer schedule SA for the preceding A lot to make the start timing for the succeeding transfer schedule SB become earlier than the end timing for the transfer schedule for the preceding A lot, so that the transfer schedule SA and the transfer schedule SB are executed in parallel, thereby improving the throughput a wafer transfer process.